REMARKS

The Examiner is thanked for conducting a personal interview with Applicant's representative on July 7, 2009. Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Claim Objection

With respect to the objection to claim 1, the Examiner suggests replacing "integrated circuit" in claim 1, line 14 with "integrated circuit, and wherein at least one of the first, second, or third step utilizes an EDA system" in order to positively tie-in the apparatus aiding in performing the method. In response, the Examiner is thanked for the suggestion. However, Applicant respectfully requests the Examiner to cite an authority (i.e., law or rule) requiring a step in a method claim to positively tie in the apparatus aiding in performing the method. Without an authority supporting the objection, Applicant would respectfully request reconsideration and withdrawal of the objection to claim 1.

Further, although the Examiner points to paragraphs [0039] and [0040] of the present application (i.e., US 2005-0120318), Applicant is unclear what and EDA system. Accordingly, Applicant respectfully requests the Examiner to clarify the meaning of EDA.

2. Rejection under 35 U.S.C. §102(e)

With respect to the rejection of claims 1-5 under 35 U.S.C. §102(e) as being anticipated by Weaver, Jr. (US 2004/0230933 – hereinafter Weaver), Applicant respectfully traverses the rejection for the record at least for the reason that Weaver fails describe each and every limitation recited in the rejected claims.

According to the present invention, a method of designing semiconductor ICs comprises two separate routines, as shown in Fig. 2 of the application. According to Fig. 2, a first routine SUB1 is a circuit design routine. Following the completion of the circuit design routine is a layout design routine SUB2.

As previously amended in accordance to the Examiner's excellent suggestions, the

presently claimed invention has been further clarified by claim 1 as directed to the circuit design routine SUB1, which is shown in details as substeps (e.g., SS16, SS20, SS22, and SS24) in Fig. 3, while dependent claim 2 has been further clarified as directed to the sequential layout design routine SUB2 shown in details as substeps (e.g., SS34, SS36, SS38, SS40, and SS42) in Fig. 4.

Applicant respectfully submits that the steps in SUB1 in Fig. 3 are performed before the steps in SUB2 in Fig. 4. Hence, the claimed steps 1st through 7th steps in claims 1 and 2 are performed in proper order as recited in the claims.

With Applicant's claimed method as recited in the steps of claims 1 and 2, for example, timing analysis is performed using the plural clocks even in the layout design (i.e., SUB2 steps) to make decision as to whether violation of timing constraints has occurred, thereby making it possible to obtain layout design that has satisfied all constraints, as discussed in lines 3-8 in page 20 of the specification.

Applicant respectfully submits that Weaver does not follow the sequential or even logical order or include the combination of steps as Applicants' claimed invention.

Weaver generally describes an IC design methodology that apply manual pre-placement (i.e., layout) of certain critical circuit elements followed by circuit optimization based on timing estimates at an early stage in the design process.

As described in, e.g., paragraph [0014] of Weaver, the pre-placement process may involve locating and fixing strategic electrical infrastructure such as clock trees, ESD protection circuits, I/O circuit, etc followed by automatic placement (i.e., layout) of the remainder of the chip circuits. The methodology of Weaver with pre-placement of critical electrical infrastructure (i.e., physical system layout) prior to a design phase is shown in, the only one drawing Fig. 1 of Weaver.

In the rejection, the Examiner contends that Applicant's claimed 2nd step for allocating clocks supplied to respective circuit is anticipated by Weaver's "element 6". That is, as contended by the Examiner during the interview, "element 6" of Weaver is interpreted as a circuit design step and not a layout design step. In response, Applicant respectfully submits that it is incorrect to interpret block 6 of pre-placement of critical circuits as a circuit design step, and such an interpretation is contrary to the teaching of Weaver.

Again, Applicant's claimed 2nd step is a step a method of designing semiconductor

ICs that includes two separate routines, and, as shown in Fig. 2 of the application, the 2nd step is a part of a first routine SUB1, which is a circuit design routine. As mentioned previously, according to the claimed invention, following the completion of the circuit design routine (i.e., SUB1) is a layout design routine (i.e., SUB2).

In contrast with Applicant's 2nd step in the design routine, Weaver's "element 6" is related to the pre-placement (i.e., layout) of critical electrical infrastructure (i.e., physical system layout). According to Weave, "element 6" performing a pre-placement or layout design step is an unconventional step in the midst of a circuit design phase, which begins in block 2 in Fig. 1 of Weaver.

Further, in Weaver there is "element 8" that provides a repeat of the pre-placement process 6 based on the condition of whether congestion is acceptable or not. This conditional repeat does not exist in Applicant's 2nd step. Therefore, Applicant respectfully submits that there is no claimed step in the present invention that remotely suggests or is equivalent to the manual pre-placement of critical electrical infrastructure in "element 6" of Weaver.

Applicant respectfully directs the Examiner's attention to, e.g., paragraph [0034] of Weaver describing the pre-placement (i.e., layout) step in a circuit synthesis/design that begins in block 2 and continues in, e.g., block 10 and thereafter.

Further, Applicant respectfully directs the Examiner's attention to paragraph [0045], which states that after the circuit design phase, the placed netlist (i.e., designed and optimized circuit) may be provided to a layout vendor, which then does a full layout design of the completed designed and optimized netlist.

Further, according to Weaver's paragraph [0014], employing a layout design step (i.e., pre-placement of critical circuits) in an early stage of a circuit design phase is advantageous because predictability of results is improved. That is, by performing a layout step (i.e., block 6) during the circuit design phase, problems with the critical components placement can be detected and solved early in circuit design. Thus, when a completed circuit design is provided to a layout vendor for a full layout, less problems and less redesign of circuit can be expected.

In another misinterpretation of Weaver, the Examiner contends that "element 18", which is performed after the design process shown in elements 4, 6, 10, 14, and 16, correspond to Applicant's layout sign process. However, Weaver specifically labels "element 18" as "route and parasitic extraction", which precedes "static timing analysis"

block 20.

Further, as discussed above, "element 6" of Weaver is not a design step/process as elements 4, 10, 14, and 16. Instead, "element 6" is a layout step/process that is uniquely performed within Weaver's design process.

Moreover, Applicant respectfully asserts that there is no relationship between the "static timing analysis" block 20 of Weaver to Applicant's 4th step for generating clocks different in delay amount for the verification of a layout design.

Further, although Weaver shows a decision block 22 determining whether or not timing is met, there is no disclosure of adjusting skews and adjusting delays, as recited in Applicant's 5th and 6th steps, respectively.

Still further, the Examiner contends that "elements 10 and 22" of Weaver are equivalent to Applicant's 3rd step as well as 5th and 6th steps. However, Applicant's 3rd step is not interchangeable or equivalent to the 5th and 6th step. Hence, such a contention by the Examiner does not appear to be logical.

Applicant respectfully reiterates that, although Examiners are entitled to interpreting a reference broadly, the reference's teaching may not be taken out of context such that its original functionality is misapplied, such as in the case of the improper application/interpretation of Weaver.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in Weaver, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-5, under 35 U.S.C. §102(e), as anticipated by Weaver is improper.

In view of the arguments set forth above, Applicant respectfully requests the Examiner to consider Weaver in its entirety as set forth in MPEP 2141.02(VI) when applying Weaver in the §102(e) rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §102(e) rejection of claims 1-5.

3. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-5 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Respectfully submitted,

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